FORM PTO-1449 (REV. 6-89)	U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office	Attorney's Docket No. 16787-06114	Serial No. 09/922,371
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant: Ajay Naini et al.	
		Filing Date: August 2, 2001	Group Art Unit: Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MM'	Q	Robert E. Goldschmidt, "Applications of Division by Convergence", *Paper submitted for Master of Science Degree, Massachusetts Institute of Technology*, June, 1964, pgs. 1-44
	R	American National Standard, "IEEE Standard for Binary Floating-Point Arithmetic", *IEEE Standard 754*, 1985, pgs. 1-14
	S	Israel Koren, "Computer Arithmetic Algorithms", *Binary Floating-Point Numbers, Fast* Addition, Chapters 4, 5, 1993, pgs. 45-98
	T	SPARC International, Inc., "The SPARC Architecture Manual, Version 9", 1993

EXAMINER: MM' DATE CONSIDERED: 1/2004

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO-1449

FORM PTO-1449 (REV. 6-88)

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

OIPE JC68 JAN 08 2002 PATENT & TRADEMARK OFFICE

Attorney's Docket No.	Serial No.
16787-06114	09/922,371
Applicant	
Ajay Naini et al.	
Filing Date	**Group Art Unit**
August 2, 2001	Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

ilm	F	Stuart F. Oberman and Michael J. Flynn, "Division Algorithms and Implementations", *IEEE Transactions on Computers*, Vol. 46, No. 8, August 1997, pp. 833-854.
	G	C.V. Ramamoorthy et al., "Some Properties of Iterative Square-Rooting Methods Using High-Speed Multiplication", *IEEE Transactions on Computers*, Vol. c-21, No. 8, August 1972, pp. 837-847.
	H	E. M. Schwartz, et al., "CMOS Floating-Point Unit for the S/390 Parallel Enterprise Server G4", *IBM Journal of Research & Development*, Vol. 41, No. 4/5, pp. 1-17, April 10, 2001.
	I	Michael J. Schulte and Earl E. Swartzlander, Jr., "A Family of Variable-Precision Interval Arithmetic Processors", *IEEE Transactions on Computers*, Vol. 49, No. 5, pp. 1-11, May 2000.
	J	Andrew D. Booth, "A Signed Binary Multiplication Technique", *Quart. Journ. Mech. and Applied Math.*, Vol. IV, Pt. 2, pp. 236-240.
	K	Christopher Williard, "Superdome – Hewlett-Packard Extends its High-End Computing Capabilities", *IDC*, pp. 1-20, 2000.
	L	Eric M. Schwartz, "Rounding for Quadratically Converging Algorithms for Division and Square Root", *Conference Record of The Twenty-Ninth Asilomar Conference on Signals, Systems and Computers*, pp. 600-603, October 30, 1995.
	M	Debjit Das Sarma and David W. Matula, "Measuring the Accuracy of ROM Reciprocal Tables", *11th Symposium on Computer Arithmetic*, pp. 95-102, June 29, 1993.
	N	Robert K. Yu and George B. Zyner, "167 MHz-4 Floating Point Multiplier", *12th Symposium on Computer Arithmetic*, pp. 149-154, July 19, 1995.
	O	Mark R. Santoro, et al., "Rounding Algorithms for IEEE Multipliers", *Proceedings, 9th Symposium on Computer Arithmetic*, pp. 176-183.
V	P	C. S. Wallace, "A Suggestion for a Fast Multiplier", *IEEE Transactions on Electronic Computers*, pp. 14-17, February 1964.

EXAMINER ilm DATE CONSIDERED 1/2004

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

OIPE
AUG 27 2001
PATENT & TRADEMARK OFFICE

FORM PTO-1449 (REV. 6-89) U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Attorney's Docket No.	Serial No.
16787-06114	09/922,371
Applicant: Ajay Naini et al.	
Filing Date: August 2, 2001	Group Art Unit: Unassigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Mm	A	E. Hokenek, et al., "Leading-zero anticipator (LZA) in the IBM RISC System/6000 Floating Point Execution Unit", IBM J. Res. Develop., Vol. 34, No. 1, January 1990
	B	Hiroaki Suzuki et al., "Leading-Zero Anticipatory Logic for High-Speed Floating Point Addition", IEEE Journal of Solid-State Circuits, Vol. 31, No. 8, August 1996
	C	Nhon T. Quach, et al., "An Improved Algorithm for High-Speed Floating-Point Addition", Technical Report: CSL-TR-90-442, August 1990
	D	A. Beaumont-Smith et al., "Reduced Latency IEEE Floating-Point Standard Adder Architectures", Department of Electrical and Electronic Engineering, University of Adelaide, Australia, August 1999, pgs. 35-42
V	E	Ajay Naini, et al., "1-GHz HAL SPARC64/sup R/Dual Floating Point Unit with RAS Features", Proceedings 15th IEEE Symposium on Computer Arithmetic. ARITH-15, 2001, pgs. 173-83

EXAMINER [signature] DATE CONSIDERED 11/2004

EXAMINER: Initial if references considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

PTO-1449